Defense Threat Reduction Agency

DTRA-NASA Radiation Hardened Microelectronics Program

Quarterly Progress Report: July 1, 2007 – September 30, 2007

End of FY07 Compendia Report

RADIATION EFFECTS ANALYSIS AND TEST PROGRAM

Report from: **NASA/GSFC**
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3.0 REQUIREMENTS (TASKS):

3.1 Task 1 - DTRA RHM Program Planning and Support:

The purpose of this task is to assist in the development and implementation of the DTRA RHM Program through the identification of critical issues, program reviews and coordination of NASA activities.

3.2 Task 2 - Characterization of Single-Event-Effect (SEE) Response of Silicon-Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) and Advanced Mixed-Signal Technologies:

The objectives of this task are to:

3.2.1 – Perform radiation testing and characterize the pre- and post-radiation response of SiGe and other advanced mixed signal technologies. This includes evaluation of test structures developed under the DARPA RHBD Program, other DARPA programs, NASA's Radiation Hardened Electronics for Space Exploration (RHESE) program, as well as advanced commercial developments.

3.2.2 - Continue to model and evaluate the performance of SiGe HBT technology including: IBM, Jazz, TI, NSC, and others. The prime focus in FY07 is to based on two aspects:

- Scaled feature size (90nm and below), and,
- Commercial product tolerance (focus on TI SiGe on SOI technology, for example)

3.2.3 – Continue to develop a high speed testing capability through the development of a ultra-high speed portable testing apparatus to establish a > 10 Gbps capability. Next generation test architectures for the 40 Gbps regime will also be explored.

The data and models generated by this task shall be used to: (1) support on orbit predictions; (2) develop a radiation effects data base for this advanced technology; (3) support the development of SEE and damage models for HBTs, (4) develop a physics based understanding of upsets in this technology and (5) support the development of radiation hardening methods.
The technical approach will include the identification and modeling of upset mechanisms, SET predictions and model validation through heavy ion and proton testing. The results of the testing shall be documented and used to support the use of these devices for space applications.
Additionally, as part of a multi-year effort, the test results will also be used to develop radiation testing protocols and predictive approaches for these technologies. This effort will be implemented through collaboration between NASA, the Georgia Institute of Technology and Auburn University.

3.3 Task 3 - Development, Demonstration and Validation of a Radiation Effects Simulation System (RADSAFE):

Development, Demonstration and Validation of a Radiation Effects Simulation System

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Purpose:

The objective of this task is to develop a physics based simulation system that is capable of SEE track modeling that can address both average and atypical device responses based on the available GEANT4 geometry and tracking code. The GEANT4 code provides a simulation tool that for the first time is capable of modeling a diverse set of nuclear reactions that include gamma radiation, cosmic rays, implant energy ions and slow neutrons. This will allow for the creation of realistic radiation event simulations not previously obtainable. This simulation system will then be used in the development of ultra-deep submicron ICs and to predict device response.

The technical approach shall include the development of the simulation system and its validation through heavy ion, proton and neutron testing to confirm modeling predictions.

The system will be fully documented and this documentation provided to DoD organizations and their contractors. This effort will be accomplished in collaboration with Vanderbilt University and the Naval Surface Warfare Center (NSWC), Crane Division.

Background:

When microelectronic and photonic components are exposed to radiation, the radiation transfers some of its energy to the component materials, significantly altering component functionality and/or parametrics. The end result depends on the type of radiation, where the energy deposition occurred, and the type of component. In general, radiation effects in microelectronic and photonic components (herein after referred to as components) can be analyzed in terms of their prompt response to ionization (generally called Single-Event Effects or SEE), and their cumulative degradation in response to the Total Ionizing Dose (TID) and Displacement Damage Dose (DDD).

Space flight mission safety and reliability rely on accurate assessment of microelectronic component response to the radiation environment. The success of radiation-effects analysis depends on several factors: 1) A conservative model of the radiation environment for evaluating the extent to which radiation threats may compromise mission goals. 2) Measurements of component responses to terrestrial radiation sources for bounding on-orbit device performance. 3) A comprehensive physical model to predict the energy deposited in the semiconductor by terrestrial and space radiation sources. 4) Physics-based component response models to predict and analyze electrical performance degradation. Existing models, developed circa 1980, make simplifying assumptions that have resulted in decreased accuracy and increased risk as

semiconductor technologies have evolved. Existing engineering models fail to estimate radiation reliability and safety accurately for important modern technologies (see section 1.1.3), leading to significant risk when these technologies are used in spacecraft.

These trends in technology developments — and the fact that the availability and affordability of powerful computers now make it possible to apply physics-based software tools that would have previously been too time-consuming for routine use — demonstrate both the need and feasibility of developing models and techniques that provide greater fidelity and flexibility for handling the broad range of current and future technologies used for spaceflight. RADSAFE (Radiation Reliability and Safety of Critical Flight Systems Using COTS and Emerging Technologies) will be a TCAD-based computational system that utilizes the best available physics, implemented by robust algorithms, enabled by supercomputer technology, and calibrated by experimental data, for predicting and analyzing the radiation response of electronic devices, circuits, and systems.

The RADSAFE concept is intrinsically modular and serial. The modules are 1) radiation environment, 2) radiation transport through the spacecraft and shielding materials, 3) radiation event generation inside the device and 4) electrical response of the device to an ensemble of events. Each module has independent routines that are exercised; the result is passed, serially, from one module to the next. The RADSAFE concept combines these models into a single platform. The development will occur in three spirals: 1) research and development of the individual modules and rudimentary integration, 2) formal development of modules and automated integration for selected technologies, including CMOS configuration circuitry for FPGAs, and 3) general-purpose automated integration and application to various technologies, including high performance digital and mixed-signal COTS and other emerging technologies.

The specific and immediate need is to develop SEE techniques. We have selected SET/SEU optodiodes as the first technology that must be modeled. Improvements in SEE prediction methods for optodiodes will allow for more accurate prediction techniques in general. The optodiode studies will be followed by SRAM and FPGA studies. This will in turn enable reliable insertion of emerging technologies like Silicon-On-Insulator, SDRAMs, and SiGe. Current methods either over predict or under predict the failure rate of these three technologies by more than an order of magnitude.

Quarterly Progress:

- **SEU and MBU model development in scaled CMOS**
  - Texas Instruments (TI) 90 nm CMOS SRAM Process
    - Built TCAD model of sensitive volume and metalization for MRED analysis of neutron data provided by TI
    - Model of 42 SRAM cells in reasonable agreement with experimental measurement of SEU and MBU
  - Developed SEU model of Sandia's 0.5 μm bulk CMOS6r 16 Kbit SRAM
    - Calibrated model with normal incidence low energy test data from BNL and minimal fabrication information
    - Successfully predicts angular dependence of direct ionization SEU for low and high energies
- **Began development of experimental set-up for SEE testing of Texas Instruments (TI) 65 nm CMOS SRAMs**

- **Began development of direct proton ionization simulations in highly scaled CMOS devices**
- **SEL modeling of TI 65 nm CMOS technology**
  - Showed SEL dependence is a 3-dimensional problem with regard to the incident particle angle of incidence
  - Showed SEL sensitivity depends on strike distance from n-well contact
  - Developed capability to model the full SRAM using TCAD
- **SEU rate calculation for SiGe 3-D shift register stage**
  - Evaluated galactic cosmic ray (GCR) and low earth orbit (LEO) upset rates for baseline and rad-hardened register stage
  - Based on charge collection efficiency model of IBM 5HP SiGe HBTs and model of cell layout
- **Single Event Gate Rupture (SEGR) Model**
  - Work was initiated to develop an RC network-based analytical model for SEGR in power MOSFETs.
    - Background information on operation of power MOSFETs, heavy ion strikes in SiO_2/Si structures, and circuit simulators such as SPICE was reviewed.
- **New MRED simulation flow**
  - Incorporates MRED radiation transport capability with a SPICE circuit simulator
    - "Critical charge" parameter no longer needed for single event cross section and rate calculations

- **Publications**

–R. A. Reed, *et al.*, "Impact of ion energy and species on single event effects analysis," *IEEE Trans. Nucl. Sci.*, accepted, 2007.
–P. E. Dodd, et. al "Impact of Heavy Ion Energy and Nuclear Interactions on Single-Event", IEEE Trans Nucl. Sci., to be published in December 2007.
–K. M. Warren, *et al.*, "Modeling alpha and neutron induced soft errors in static random access memories," in *Proc. Int. Conf. IC Design & Technology*, Austin, TX: IEEE, May 2007.
–K. M. Warren, *et al*., "Predicting thermal neutron-induced soft errors in static memories using TCAD and physics-based Monte-Carlo simulation tools," *IEEE Electron Device Lett.*, vol. 28, pp. 180-182, Feb. 2007.
–K. M. Warren, *et al*., " Monte-Carlo Based On-Orbit Single Event Upset Rate Prediction for a Radiation Hardened by Design Latch" IEEE Trans Nucl. Sci., to be published in December 2007.
–C. L. Howe, et. al "Distribution of Proton-Induced Transients in Silicon Focal Plane Arrays," IEEE Trans Nucl. Sci., to be published in December 2007.
–J. A. Pellish, et al., "A generalized SiGe HBT single-event effects model for on-orbit event rate calculations," IEEE Trans. Nucl. Sci., accepted, 2007.
–J. M. Hutson, *et al.*, "The effects of angle of incidence and temperature on latchup in a 65 nm technology," *IEEE Trans. Nucl. Sci.*, accepted, 2007.
–M. J. Gadlage, *et al*., "Assessing alpha particle-induced single-event transient vulnerability in a 90 nm CMOS technology," *IEEE Electron Device Lett.*, submitted.

Work Planned for Next Quarter:

- **Development of model for 65 nm TI CMOS technology**
    - Create process and design model for MRED
    - Examine impact of angular dependence on error rate
    - Support testing of TI SRAMs
- **Continue development of test boards to perform SEU, MBU and SEL experiments on TI 65 nm CMOS SRAMs.**
- **Develop a plan to address the impact of direct ionization from protons on modern technology**
- **SEL modeling for 65 nm TI CMOS technology**
    - Use TCAD model to map potential drops in the N-well and flag possible latching events
- **Continue transient testing of SiGe HBTs with laser in order to understand event durations**
- **Continue development of analytical SEGR model**
- **Begin work to define a metric for estimating the contribution of nuclear reactions to on-orbit SER from ground based test data**

Milestones/Deliverables:
None

3.4 TASK 4 – Test and Evaluation of the Radiation Response of Commercial and Hardened Microelectronics:

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Purpose:

The objective of this task is to test and evaluate the radiation response of various commercial and hardened near and state-of-the art microelectronics technologies and devices including ultra-deep-submicron test structures, FPGAs/high-speed, and memories.

The results of the testing shall be documented and used to support the use of these devices/technologies for space applications. Additionally, as part of a multi-year effort, the test results will also be used to develop radiation testing protocols and support hardened devices under development.

The specific goals for the FY07 effort that include:

(1) Evaluation of TID, SEE/DSET and other effects radiation effects in scaled CMOS to include IBM (90nm – in support of the DARPA RHBD Program), TI (130, 90, 65,

and 45 nm w/Vanderbilt), IMEC (65nm), Jazz (TBD) and other state-of-the –art commercial technologies.

(2) Investigation of selected non-volatile and volatile storage technologies to include (as available) carbon nanotube (Nantero, BAE), MRAM (Honeywell, Freescale), commercial Flash (<=90nm from Samsung, Toshiba, Micron, STM, and volatile memories to include 512Mb/1Gb+ SDRAMs (Samsung, Elpida). New hardening approaches will be evaluates as available.

(3) Utilization of <=90nm FPGAs for commercial device performance in a radiation environment This includes Xilinx 90 and 65nm devices. Focus will be on geometric and temporal effects. Additional evaluation of high-speed devices (SERDES, fiber optic links) will also be considered.

Background:

Deep sub-micron processes are now available in the market. Their performances are very attractive for space designers. Based on previous work published, we expect these technologies to have a good Total Dose Tolerance. The main concerns are the SEEs, especially the DSET. The testing of these state of the art technologies poses a lot challenges: complexity of the functions to test, high speed, packaging issues.

Annual Progress:

- Non-Volatile Memories (NVM) - Flash memory
    - Performed total dose and heavy ion tests on Samsung 4G NAND flash (63 nm technology). All parts passed TID at 100 krad (SiO_2), seven of eight passed at 150 krads (SiO_2), and failed at 200 krad (SiO_2). Static bit error rate, calculated with CREME96 for geosynchronous orbit at solar minimum, is about $1x10^{-12}$ errors/bit-day.
    - STM 1Gbit 90nm samples were tested for TID and HI SEU response. Parts failed TID between 30 and 100 krads (SiO_2). In the heavy ion test, the SEFI rate was high enough that it was difficult to determine a bit error rate.
    - Obtained 4G NAND flash samples from SWRI for Micron and Hynix, and performed TID and heavy ion testing. Hynix parts failed TID 30-75 krads (SiO_2). Micron parts failed TID 75-150 krads (SiO_2). The SEFI rate was high enough that it was difficult to determine a bit error rate for either Micron or Hynix.
    - Samsung, Hynix and Micron 4G NAND flash were tested at 70 C and 3.6V for latchup, but no latchup was observed on any sample, up to LET=55. At LET=55, other destructive effects were observed, so the test could not be continued.
    - Samsung has agreed to supply 8G single die, single level cell NAND samples.
    - All above tests have been on NAND architecture devices. NOR devices will also be evaluated in FY08.
        - Additional endurance testing being considered.
- NVM – other
    - FRAMs (ferroelectric)
        - TI/Ramtron 4 Mb devices
            - Heavy ion and proton SEE tests completed. Data analysis underway. Report expect in 1Q FY08
                - Results encouraging enough to perform TID in FY08
        - Fujitsu 4 Mb
            - Heavy ion testing showed significant SEL susceptibility. Data analysis underway, but no further testing planned.
    - EEPROM
        - MEMTEK startup devices evaluated for heavy ions. No SEL or stuck bits encountered. Test report due in 1Q FY08. Plans to perform TID in FY08.
    - MRAM
        - TID testing performed on Freescale commercial 4 Mb MRAM
            - ~100 krads-Si of tolerance noted
            - Test report due in 1Q FY08
            - JPL to perform SEE tests via NASA funding.
    - Carbon nanotube
        - No devices delivered/available

- Phase Change
  - No devices delivered/available

- SDRAMs
  - Completed SEE and proton SEE testing of Samsung and Elpida 1 Gb DDR2 SDRAMs. These are 90nm CMOS (bulk) devices.
    - Samsung performed significantly better than Elpida in terms of SEFI performance. No SEL observed at 85C.
    - Samsung devices showed no degradation with 100 krads-Si of protons
    - Data presented at NSREC
  - Began planning for TID testing of DDR2 SDRAMs for FY08
  - Ordered Micron DDR2 devices capable of internal 1.066 GHz operation
  - Biggest challenge has been deprocessing the devices for heavy ion testing and limitations due to materials for angular tests.
    - Radiation Assured Devices (RAD) has been our prime organization hired to deprocess.

- SRAM
  - Performed heavy ion tests on rad-tolerant Renesas SRAM
    - Data analysis underway. Test report due in 1Q FY08
    - Navsea performed DR tests and TID
  - ST Micro SRAM samples still being discussed

- IBM
  - Obtained working agreement with IBM to support technology evaluation
  - Performed proton SEE testing using 60-200 MeV protons on 65nm "HOMER" SOI SRAMs (8 designs)
    - Data analysis underway, but tolerance to TID looked promising, no SEL observed. SER under analysis.
    - Note: IBM will release reports to DTRA directly due to IBM lawyers
  - Heavy ion and preliminary proton (4-60 MeV looking for direct ionization) SEE tests planned for 1Q FY08
    - TID testing will follow pending sample availability
    - Angular tests are among key aspects.
    - Sandia performing high energy proton and neutron tests collaboratively.
  - Discussing evaluation of CELL processor and other structures to llok at more complex effects. CELL is very low power and could be of considerate interest.

- Xilinx/TSMC – Transistors
  - Completed report on 90nm Xilinx/TSMC bulk transistors using standard IV techniques
    - Report available on radhome website, but little degradation noted
  - Prepared 65nm Xilinx/TSMC bulk transistors for TID test campaign in FY08
    - 1st test is standard IV test at room temp
      - Initial results show little degradation at 1.7 Mrad-Si (highest dose tested)
      - Analysis underway

        - 2nd test will utilize pulsed IV techniques (edge effects?)
        - 3rd test will perform characterizations over Mil-Temp range to determine if room temperature tests accurately demonstrate conservative results
- TI/Vanderbilt – Test Structures
    - Space Act Agreement in place between NASA and TI. All data considered FOGUO
    - 65nm bulk transistor testing is awaiting packaging by Vanderbilt. Plan to test in manner similar to TSMC transistors.
    - 65nm bulk SRAMs diced and being put into test assembly using chip-on-board (COB) technique via RAD.
        - 1st board spin had connector rows reversed. Board is being re-spun.
        - Heavy ion test scheduled for Nov 08. Proton is TBD.
            - Focus is on angular effects
- IMEC
    - Completed 65nm transistor TID testing
    - Report available on radhome website, but sample size and yields were poor and data interpretation is limited.
- Intel
    - Performed TID and dose rate (DR) tests in collaboration with Intel and Navsea-Crane on 65nm dual core E6850 processor
        - Data is considered FOGUO and proprietary to Intel
        - TID: No degradation noted at 1 Mrad-Si
            - Full parametric characterization performed by Intel
        - DR: No upset or latchup noted to1E9
            - Upsets noted beyond this level, but are thought to be caused by external temperature detection circuitry
            - Navsea is finalizing test report
        - Plans for 45nm hi-K devices in FY08.
- Boeing
    - Supported 150nm and 90nm SEE tests at LBNL by Boeing using FPGA-based tester for DTRA/DARPA RHBD and UDSM programs
        - Reports from Boeing Phantomworks.
- Freescale
    - Continued discussion on getting samples to test
        - Limited progress
- Broadcomm
    - Met with Broadcomm and had initial interest in scaled CMOS samples for hi-rel evaluation
        - This was halted by Broadcomm due to financial/legal issues
- Ultra-low power (ULP)
    - Testing of 65nm ULP ADC did not gather relevant SEE data
        - Delidded device proved to be too noisy in test fixture to gather data in a reliable manner
    - MIT-LL has delivered a Digital FIR evaluation board
        - We hope to perform radiation testing in FY08, but again are concerned with noise issues

    - Are continuing discussions on ULP SRAMs which might be a more reasonable test structure to utilize
- Digital.Single Event Transient (DSET) Guidance
    - Draft document begun on testing complex commercial devices for DSET information
    - Transitioned task from Christian Poivey to Paul Marshall
- Mixed Signal – ADCs
    - Began drafting a guidance document for performing radiation tests on ADCs
        - This subtask is behind schedule due to resource (personnel) issues
        - Draft is under review
    - Coordinated plans with both TI and NSC for evaluation of perspective space market ADCs
        - TI's is SiGe on SOI (AD5424). Initial test plans fell through due to h/w issues
        - Initial heavy ion tests planned for Nov 08 on both
- Mixed Signal – LVDOs
    - Completed tests and reports on devices tested in FY06
- Mixed Signal – Foundry Variation and Cold Storage
    - Supported TID evaluation by TI on Unitrode products that have shown foundry site (same process?) to foundry site variation
        - Utilized dry nitrogen storage post-irradiation as a means to extend time between irradiation and measurement
            - FY08 will look at this technique for multiple technology nodes
        - TI has reports available
- TID Impact on SEE Performance
    - Supported combined TID irradiation with LASER and heavy ion tests on LM124 collaboratively with Univ of Montpelier and NRL
        - Montpelier focused on changes in SEE response as indicator of failure mechanisms. Presented by M. Bernard at NSREC
        - NASA focused on changes in SEE response as RHA concern for designs. Presented by S. Buchner at RADECS.
    - FY08 will look at parts from differing technologies as a survey of the impact of this concern.
- FPGAs
    - Xilinx
        - Full device characterization performed on 90nm Xilinx Virtex-IV FX60 with dual processor for a flight project leveraging techniques developed by this task in FY06
            - Part > 300 krads-SI, no SEL
            - Very SEU sensitive
                - Study comparing types of error modes as well as evaluating limited mitigation techniques performed
        - XIlinx Virtex-IV 90nm FPGAs evaluated focusing on scrubbing and hidden errors due to bean flux/scrubbing

        - I.e., does SEFI or configuration error hide errors occurring in logic and how do you measure the logic sensitivity?
        - 65nm devices being considered for FY08
- Aeroflex
    - Investigated anomalous SEU data on Eclipse devices showing *decrease* in SEU cross-section with increasing speed
        - We are working directly with Aeroflex to understand cause (circuit design?, drive?, …) and will likely perform further tests in FY08
- Actel
    - Supporting RTAX-S evaluation by CPSG based on FY06 RTAX-S test techniques and results
- Atmel
    - Awaiting delivery of 300 kgate RAM-based rad-tolerant FPGA
        - FY08 expectation now
- Achronix/BA FPOA
    - Performed initial Heavy Ion SEE test
        - Data analysis underway further tests planned
- Honeywell/Mathstar FPOA
    - Began discussions for future radiation tests

Milestones/Deliverables:

- Test reports

3.5 TASK 5 – Test and Characterization of the Radiation Induced Response of Sensors Technology:

This task does not exist in FY07.

3.6 TASK 6 – Development of a High Speed Radiation Test Apparatus and Method:

This task does not exist in FY07.

3.7 TASK 7 – Test Facility Support:

The objective of this task is to provide radiation test facility support for various DTRA RHM Program deliverables. The test facility time (without overhead) is as follows:

1. TBD

The results of the testing shall be documented and used to support the application of these devices for space applications.